What is claimed is:

1. A method of manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor substrate on which a given process is implemented in order to form a semiconductor device;

forming an ion implantation layer by means of an ion implantation process; and

controlling the impurity concentration of the ion implantation layer by means of a cleaning process.

2. The method as claimed in claim 1, wherein the ion implantation layer is formed by implanting an impurity of 1E11 ~ 1E13 ion/cm_2 with energy of 5 ~ 50keV.

3. The method as claimed in claim 2, wherein the impurity is boron.

4. The method as claimed in claim 2, wherein the impurity is implanted at an angle of 3 ~ 13° .

5. The method as claimed in claim 1, wherein the cleaning process is implemented using a solution of fluoric acid series and wherein the concentration of the impurity is reduced by out gassing the impurity.

6. The method as claimed in claim 5, wherein the solution of a fluoric acid series employs diluted HF in which H_2O:HF is mixed in the ratio of 1:1 ~ 50:1 as an undiluted solution.

7. The method as claimed in claim 1, wherein the cleaning process controls the concentration of the remaining impurity by controlling the concentration of the solution or the progress time.

8. The method as claimed in claim 1, wherein during the cleaning process, a SC-1($NH_4OH/H_2O_2/H_2O$) solution is added together to remove a native oxide film on the surface of the semiconductor substrate, so that out gassing of the impurity is activated.

9. The method as claimed in claim 1, further comprising the steps of after the concentration of the impurity is controlled,

sequentially forming a tunnel oxide film and a first polysilicon layer over a semiconductor substrate and then implementing patterning;

forming an isolation film in an isolation region of the semiconductor substrate;

sequentially forming a dielectric film, a second polysilicon layer and a silicide layer on the entire structure of the semiconductor substrate;

sequentially patterning the silicide layer, the second polysilicon layer and the dielectric film by means of an etch process using a control gate mask;

patterning the first polysilicon layer by means of a self-aligned etch process; and

forming source/drain in the semiconductor substrate around the first polysilicon layer.

10. The method as claimed in claim 9, wherein the source/drain has a DDD junction structure.